(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 991 268 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
05.04.2000 Bulletin 2000/14

(51) Int Cl.[7]: **H04N 5/232**

(21) Application number: **99307645.4**

(22) Date of filing: **28.09.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.09.1998 JP 27401198**

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka 571-8501 (JP)

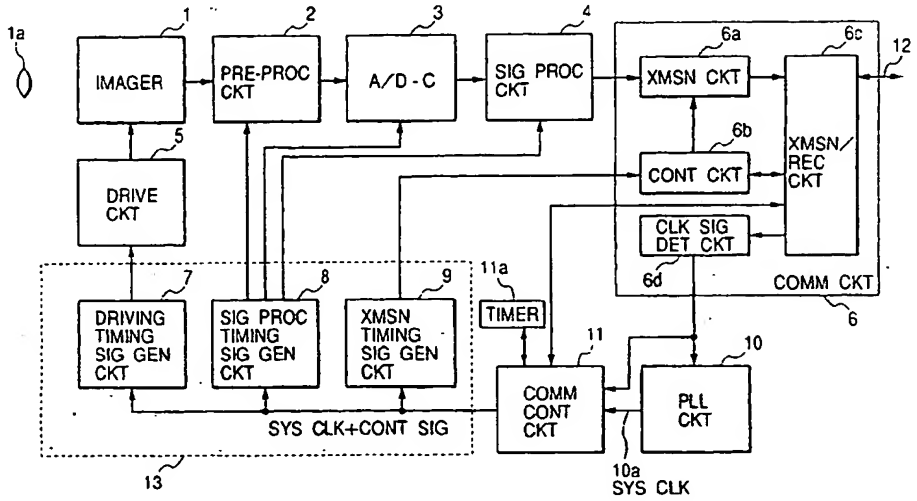
(72) Inventor: **Shinohara, Toshiaki**
Oomiya-shi, Saitama-ken 330-0038 (JP)

(74) Representative: **Senior, Alan Murray et al**
J.A. KEMP & CO.,
14 South Square,
Gray's Inn
London WC1R 5LX (GB)

(54) An imaging apparatus with video data transmission

(57) A communication circuit transmits the digital video signal to a transmission line and receives a clock signal and timing data transmitted through the transmission line. The timing data indicates a communication timing. A timing signal generation circuit generates timing signals from the detected clock signal to control the imager, the a/d converting circuit, the signal processing circuit, and the communication circuit. A communication control circuit detects a communication timing from the timing data, judges whether the communication timing is detected within a predetermined condition (communication error), and controls the timing signal generation circuit to stop transmitting the digital video signal when the communication timing is not detected within the predetermined condition to prevent a fail in transmitting the video data. A shutter interval of the imager is further controlled toward a constant shutter interval in response to the communication error. The video signal is stored in a memory in response to the communication error and read if the communication error eliminated. The communication error is displayed. A system control signal indicative of data transmission period is generated in response to a received cycle start packet in accordance with the obtained data rate and channel timing.

FIG. 1



EP 0 991 268 A2

Description

[0001] This invention relates to an imaging apparatus for receiving an image, generating video data from the image received by a camera, and transmitting the video data.

[0002] An imaging apparatus for receiving an image by a camera, generating video data from the received image, and transmitting the video data is known. In this prior art imaging apparatus, a clock signal is received by a transmitting and receiving circuit and the imager of the imaging apparatus is synchronously operated with the received clock signal. Such a prior art imaging apparatus is disclosed in Japanese patent application provisional publication No. 9-130655. Fig. 13 is a block diagram of a prior art imaging apparatus for receiving an image by a camera, generating video data from the received image, and transmitting the video data. The prior art imaging apparatus includes: an imager 101 for generating an image signal from the image formed by a lens 101a, a pre-processing circuit 102 for pre-processing the image signal, an a/d converter 103 for a/d-converting the image signal from the pre-processing circuit 102, a signal processing circuit 104 for processing the image signal from the a/d converter 104 to generate a digital video signal, a transmission/receiving circuit 106 for transmitting the digital video signal and extracting a clock signal from a serial signal. a PLL circuit 110 for frequency-multiplying the clock signal to generate another clock signal, a transmission/receiving timing generation circuit 109 for generating a timing signal for the transmission/receiving circuit 106, a signal processing timing generation circuit 108 for generating timing signals for the pre-processing circuit 102, the a/d converter 103, and the signal processing circuit 104, and a driving timing generation circuit 107 for generating a driving timing signal, and a driving circuit 105 for generating a driving signal for the imager 101 from the driving timing signal.

[0003] The aim of the present invention is to provide a superior imaging apparatus and to provide a superior imaging, apparatus for continuously transmitting video data without noise or disturbance in the reproduced image though the communication cycle timing is not detected temporarily

[0004] According to the invention, there is provided a first imaging apparatus including: an imager; an optical unit for receiving and forming an image on the imager which generates an image signal from the image; an a/d converter for a/d-converting the image signal; a signal processing circuit for processing the image signal from the a/d converter to generate a digital video signal; a communication circuit for transmitting the digital video signal to a transmission line and receiving a clock signal and timing data transmitted through the transmission line, the timing data indicating a communication timing; a clock signal detection circuit for detecting the clock signal received by the communication circuit; a timing signal generation circuit for generating timing signals from the detected clock signal to control the imager, the a/d converter, the signal processing circuit, and the communication circuit; and a communication control circuit for detecting a communication timing from the timing data, judging whether the communication timing is detected within a predetermined condition, and controlling the timing signal generation circuit to stop transmitting the digital video signal when the communication timing is not detected within the predetermined condition.

[0005] In the first imaging apparatus, the communication circuit may receive a communication cycle header as the timing data and the communication control circuit detects an error in the communication cycle header from the transmitting and receiving circuit and judges that the communication timing is not received within the predetermined condition when the error is detected.

[0006] In the first imaging apparatus, the communication control circuit may control the timing signal generation circuit to stop operations of the imager, the a/d-converter, the signal processing circuit, and the communication circuit when the communication timing is not detected within the predetermined condition.

[0007] The first imaging apparatus may further include a shutter controlling circuit for controlling a shutter interval of the imager in accordance with the detected clock signal when the communication timing is detected within the predetermined condition and controlling the shutter interval of the imager in response to the detected error toward a predetermined shutter interval.

[0008] The first imaging apparatus may further include a storing circuit for storing the digital video signal, wherein the communication control circuit operates the storing circuit to store the digital video signal when the communication control circuit judges the communication timing is not detected within the predetermined condition and operates the storing circuit to read the digital video signal to supply the read digital video signal to the communication circuit when the communication control circuit judges the communication timing is detected again within the predetermined condition.

[0009] The first imaging apparatus may further include a display, wherein the communication control circuit operates the display to inform that the communication control circuit judges the communication timing is not detected within the predetermined condition.

[0010] According to this invention, there is provided a second imaging apparatus including: an imager; an optical unit for receiving and forming an image on the imager which generates an image signal from the image; an a/d converter for a/d-converting the image signal, a signal processing circuit for processing the image signal from the a/d converter to generate a digital video signal; a communication circuit for transmitting the digital video signal to an external communication apparatus transmitting the timing data indicative of a communication cycle and receiving the timing data from the external communication apparatus; a clock signal detection circuit for

detecting a clock signal received by the communication circuit; a timing signal generation circuit for generating timing signals from the detected clock signal to control the imager, the a/d converter, the signal processing circuit, and the communication circuit; and a data transmission interval signal generation circuit for detecting a communication timing from the timing data and generating a transmitting interval signal indicative of a transmitting interval and a transmitting stop interval, wherein the communication circuit transmits the digital video signal only for the transmitting interval.

[0011] In the second imaging apparatus, the data transmission interval signal generation circuit detects transmission data rate data and channel data from the transmitting and receiving circuit to generate the transmitting interval signal.

[0012] In the second imaging apparatus, wherein the timing signal generation circuit stops generating the timing signals to stop operations of the imager, the a/d-converter, the signal processing circuit, and the transmitting circuit.

[0013] The second imaging apparatus may further includes a shutter interval control circuit for controlling a shutter interval of the imager toward a predetermined interval during the transmitting stop interval.

[0014] The second imaging apparatus may further include a memory responsive to the transmission interval signal for storing the digital video signal for the transmission stop interval and reading and supplying the read digital video signal to the communication circuit to transmit the read digital video signal for the transmission interval.

[0015] The second imaging apparatus may further include a further comprising a display for informing that it is during the transmission stop interval.

[0016] In the first imaging apparatus, the communication control circuit detects an error in the communication circuit, and controls the timing signal generation circuit to stop transmitting the digital video signal in the presence of the error.

[0017] In this case, the communication control circuit judges whether the clock signal is detected within a reference condition to detect the error, and controls the timing signal generation circuit to stop transmitting the digital video signal in the presence of the error.

[0018] In this case, the communication control circuit detects a communication timing from the timing data, judges whether the communication timing is detected within a predetermined condition to detect the error, and controls the timing signal generation circuit to stop transmitting the digital video signal in the presence of the error.

[0019] The aim and features of the present invention will become more readily apparent from the following detailed description of exemplary embodiments and the accompanying drawings, in which:

Fig. 1 is a block diagram of an imaging apparatus with video data transmission according to a first embodiment;

Figs. 2A to 2D are illustrations of data arrangement according to the first embodiment;

Fig. 3 depicts a flow chart of the first embodiment showing the operation of the communication control circuit shown in Fig. 1;

Figs. 4A and 4B are time charts of this embodiment showing operation of the communication control circuit shown in Fig. 1;

Fig. 5 is a block diagram of the imaging apparatus of a second embodiment;

Fig. 6 is a block diagram of the imaging apparatus of a third embodiment;

Fig. 7 is a block diagram of the imaging apparatus of a fourth embodiment;

Fig. 8 is a block diagram of an imaging apparatus with video data transmission according to a fifth embodiment;

Figs. 9A to 9C are timing charts of the fifth embodiment which are also referred in the seventh embodiment;

Fig. 10A depicts a flow chart of the transmission interval determining circuit shown in Fig. 8;

Fig. 10B depicts a flow chart of the system timing generation circuit shown in Fig. 8;

Fig. 11 is a block diagram of the imaging apparatus of a sixth embodiment;

Fig. 12 is a block diagram of the imaging apparatus of a seventh embodiment; and

Fig. 13 is a block diagram of a prior art imaging apparatus.

[0020] The same or corresponding elements or parts are designated with like references throughout the drawings.

<FIRST EMBODIMENT>

[0021] Fig. 1 is a block diagram of an imaging apparatus with video data transmission according to a first embodiment.

[0022] The imaging apparatus of the first embodiment includes: an imager 1, an optical lens la for receiving and forming an image on the imager 1 which generates an image signal from the image, a pre-processing circuit 2 for pre-processing the image signal, an a/d converter 3 for a/d-converting the image signal from the pre-processing circuit 2, a signal processing circuit 4 for processing the image signal from the a/d converter 4 to generate a digital video signal, a communication circuit 6 for transmitting the digital video signal to a transmission line 12 with a transmission circuit 6a and a transmission/receiving circuit 6c. Moreover, the communication circuit 6 receives a clock signal, a cycle start packet (timing data), and control data transmitted through the transmission line 12 with the transmission/receiving circuit 6c, a clock signal detection circuit 6d, and a control

circuit 6b.

[0023] The imaging apparatus further includes a PLL (phase-locked loop) circuit 10 for frequency-multiplying the clock signal from the clock signal detecting circuit 6e to generate a system clock signal 10a, a timing signal generation circuit 13 for generating timing signals from the system clock signal to control the imager 1, the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4, and the communication circuit 6, and a communication control circuit 11 responsive to clock signal from the clock signal detection circuit 6 and the system clock signal 10a for detecting the header from the transmission/receiving circuit 6c to detect a communication timing from the header, judging whether the communication timing is correctly detected, that is, the communication timing is detected within a predetermined condition, and controlling the timing signal generation circuit 13 to stop transmitting the digital video signal when the communication timing is not detected within the predetermined condition.

[0024] The communication control circuit 11 is further responsive to a timer lla for judging whether the communication timing is detected within the predetermined condition. That is, the communication control circuit 11 judges the communication timing becomes within a predetermined interval from the previous communication timing with the timer 11a.

[0025] The timing data indicates a communication timing and a communication cycle. The clock signal detection circuit 6d detects the clock signal received by the transmission/receiving circuit 6c.

[0026] Operation of the imaging apparatus will be described with assumption that a transmission method according to IEEE1394 is used.

[0027] Figs. 2A to 2D are illustrations of data arrangement according to the first embodiment. Fig. 3 depicts a flow chart of the first embodiment showing the operation of the communication control circuit 11.

[0028] The optical lens la receives and forms an image on the imager 1 which generates the image signal from the image. The pre-processing circuit 2 pre-processing the image signal. For example, the pre-processing circuit 2 effects the correlation double sampling, the automatic gain controlling, etc. The a/d converter 3 a/d-converts the image signal from the pre-processing circuit 2 to output a digital image signal. The signal processing circuit 4 processes the digital image signal from the a/d converter 4 to generate a digital video signal including a luminance signal Y, color difference signals U and V and effects video signal processes including the white balance adjustment, the gamma processing, etc. to output the digital video signal. More specifically, the imager 1 supplies the image signal every pixel to the transmission circuit 6a through the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4 in response to the timing signals from the driving timing signal generation circuit 7, and the signal processing timing signal generation circuit 8.

[0029] In Fig. 2A, a cycle start packet CSP is transmitted from the transmission line 12. Following to the cycle start packet CSP, a first channel (CH1) of data is transmitted. Following to the first channel (CH1) of data, a second channel (CH2) of isochronous data is transmitted from this imaging apparatus.

[0030] In Figs. 2B and 2C, it is assumed that luminance data Y, the color difference data U, and the color difference data V are transmitted at a ratio of 4: 1 : 1. The transmission circuit 6a generates a serial data train including an isochronous header ISOH at the beginning of the serial data train, the video data of a first horizontal line and the video data of second horizontal line, and error check code CR at the end of the serial data train in response to every cycle start packet CSP transmitted by a cycle master apparatus (not shown) coupled to the transmission line 12 as shown in Fig. 2B. Each line of the video data includes video data of U1, Y1, Y2, V1, Y3, Y4, U2 to Yn as shown in Fig. 2C. That is, one pieces of each color differential data U and V are transmitted every four pieces of luminance data. Two horizontal lines of video data (Fig. 2D) is transmitted in one slot of the second channel CH2.

[0031] The cycle start packet CSP includes a header and CRC data of the header as shown in Fig. 2B.

[0032] The driving timing signal generation circuit 7, the signal processing timing signal generation circuit 8, and the transmission timing signal generation circuit 9 controls the transmission timing of respective driving circuit 5, the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4, and the communication circuit 6 in response to the system clock 10a generated by the PLL circuit 10 or a clock generated by a crystal oscillator (not shown) provided in the imager 1. The communication control circuit 11 controls the driving timing signal generation circuit 7, the signal processing timing signal generation circuit 8, and the transmission timing signal generation circuit 9 when an error occurs in communication cycle timing. That is, when an error occurs in communication cycle timing, the communication control circuit 11 stops supplying the system clock 10a to the timing signal generation circuit 13 or supplying the system clock 10a but disables the driving timing signal generation circuit 7, the signal processing timing signal generation circuit 8, and transmission timing signal generation circuit 9. Moreover, it is also possible that the communication control circuit 11 directly controls the imager 1, the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4, and the transmission circuit 6a to stop their operations when the error in the communication cycle.

[0033] The transmission/receiving circuit 6c receives a multiplexed clock signal and a cycle start packet CSP transmitted through the transmission line 12. The clock signal detection circuit 6d detects the multiplexed clock signal transmitted through the transmission line 12 and generates a system clock 10a.

[0034] Fig. 3 depicts a flow chart of the first embodi-

ment showing operation of the communication control circuit 11.

[0035] The communication control circuit 11 detects the header CSPH of the cycle start packet CSP (communication cycle header) received by the transmission/receiving circuit 6c in step ST1. In the following step ST2, the communication control circuit 11 effects the CRC (cyclic redundancy check) operation to the data of the header and compares the result of the CRC operation with the CRC data added to the cycle start packet CSP to check whether there is a communication cycle error in step ST3. When there in no communication error in step ST3, that is, the communication control circuit 11 judges that the communication timing is detected within the predetermined condition, the communication control circuit 11 continues to supply the system clock 10a to the timing signal generation circuit 13 to enable operations of the imager 1, the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4, the transmission circuit 6a and the transmission portion of the transmission/receiving circuit 6c. If there is a communication cycle error, that is, the communication control circuit 11 judges that the communication timing is detected without the predetermined condition, the communication control circuit 11 stops supplying the system clock 10a to the timing signal generation circuit 13 to stop (disable) operations of the imager 1, the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4, the transmission circuit 6a and the transmission portion of the transmission/receiving circuit 6c. When the following cycle start packet is received again without communication error in step ST3, the communication control circuit 11 starts to supply the system clock 10a (enable) to the timing signal generation circuit 13 to enable operations of the imager 1, the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4, the transmission circuit 6a and the transmission portion of the transmission/receiving circuit 6c.

[0036] The communication control circuit 11 obtains one of channels, for example, channel two CH2. Then, the communication control circuit 11 transmits the serial data including the isochronous header ISOH, consecutive two horizontal lines of the video data (video signal), and the error check code CR at the timing of the channel two CH2 which is a predetermined interval after the cycle start packet CSP.

[0037] The communication control circuit 11 is further detects the communication error. That is, the communication control circuit 11 is further responsive to a timer lla for judging whether the cycle start packet CSP is detected within the predetermined interval from the previous cycle start packet with the timer 11a. Moreover, the communication control circuit 11 detects that the clock is not detected within the predetermined condition. That is, the communication control circuit 11 judges whether the clock signal is detected within a predetermined interval which is slightly longer than the clock cycle.

[0038] The cycle start packet (timing data) CSP indicates a communication timing of the obtained channel and the communication cycle.

[0039] Figs. 4A and 4B are time charts of this embodiment showing the operation of the communication control circuit 11. When the communication error, that is, there is an error in the data in the header CSPH of the cycle start packet CSP at t0, the system clock from the communication control circuit 11 is stopped, so that no video data is transmitted. When the header CSPH of the cycle start packet CSP is correctly detected again, the system clock from the communication control circuit 11 is supplied again, so that video data (digital video signal) is transmitted.

<SECOND EMBODIMENT>

[0040] Fig. 5 is a block diagram of the imaging apparatus of a second embodiment.

[0041] The structure of the imaging apparatus of the second embodiment is substantially the same as that of the first embodiment. The difference is that a communication trouble display 16 including an LED is further provided. When the communication control circuit 11 detects the communication error, the communication trouble display 16 display the occurrence of the communication error. Moreover, the communication control circuit 11 transmits the data of communication error to an external computer to check the communication quality.

<THIRD EMBODIMENT>

[0042] Fig. 6 is a block diagram of the imaging apparatus of a third embodiment.

[0043] The structure of the imaging apparatus of the third embodiment is substantially the same as that of the first embodiment. The difference is that a shutter interval control circuit 5a is further provided.

[0044] If the communication error occurs, the shutter interval will be extended because the shutter interval is controlled in accordance with the number of pulses of the clock signals or the cycle start packet CSP. To prevent the extension of the shutter interval, when the communication control circuit 11 detects the communication error, the communication control circuit 11 operates the shutter interval control circuit 5a to control a shutter interval of the imager 1 toward a predetermined shutter interval. More specifically, when the communication error is detected because the clock signal cannot be detected, a count value of a counter (not shown) for counting pulses of the system clock 10a which is supplied from the PLL circuit 10 via the communication control circuit 11 is increased by a predetermined value or a set value to be compared with the count value in the counter may be decreased by a predetermined value to make the shutter interval constant. Moreover, it is also possible that in response to start of exposure, a timer (not shown) measures a predetermined interval and the shutter closing timing is determined in accordance with

either the timer or the counter which becomes the shutter closing timing earlier to make the shutter interval constant.

<FOURTH EMBODIMENT>

[0045] Fig. 7 is a block diagram of the imaging apparatus of a fourth embodiment.

[0046] The structure of the imaging apparatus of the fourth embodiment is substantially the same as that of the first embodiment. The difference is that a FIFO (first-in first-out) memory circuit 14 and a FIFO reading/writing timing signal generation circuit 15 are further provided.

[0047] When there is no communication error, the digital video signal from the signal processing circuit 4 is immediately supplied to the transmission circuit 6a through through the FIFO memory circuit 14. On the other hand, when the communication error is detected, the communication control circuit 11 operates the FIFO reading/writing timing signal generation circuit 15 to temporally store the digital video signal from the signal processing circuit 4 and. When the communication error eliminates, the communication control circuit 11 operates the FIFO reading/writing timing signal generation circuit 15 to read the stored the digital video signal to supply the read digital video signal to the transmission circuit 6a to transmit the digital video signal to the transmission line 12.

[0048] As mentioned, if the communication error occurs, the imager 1, the pre-processing circuit 2, the a/d converter 3, the signal processing circuit 4, and the FIFO memory circuit 14 are continuously operated, so that the image represented by the digital video data is continuously transmitted.

[0049] If the communication error occurs because the clock signal cannot be detected by the clock signal detection circuit 6d, the PLL circuit 10 generates the system clock signal 10a at a lowest frequency, so that it is desirable that the shutter interval control circuit 5a mentioned in the third embodiment is provided.

<FIFTH EMBODIMENT>

[0050] Fig. 8 is a block diagram of an imaging apparatus with video data transmission according to a fifth embodiment.

[0051] The imaging apparatus of the fifth embodiment includes: an imager 21, an optical lens 21a for receiving and forming an image on the imager 21 which generates an image signal from the image, a pre-processing circuit 22 for pre-processing the image signal, an a/d converter 23 for a/d-converting the image signal from the pre-processing circuit 22, a signal processing circuit 24 for processing the image signal from the a/d converter 24 to generate a digital video signal, a communication circuit 26 for transmitting the digital video signal to the transmission line 12 with a transmission circuit 26a and a transmission/receiving circuit 26c. Moreover, the communication circuit 26 receives a clock signal, a cycle start packet (communication timing data), and control data transmitted through the transmission line 12 with the transmission/receiving circuit 26c, a clock signal detection circuit 26d, a transmission interval determining circuit 26e, and a control circuit 26b.

[0052] The imaging apparatus further includes a PLL circuit 30 for frequency-multiplying the clock signal from the clock signal detecting circuit 26e to generate a system clock signal 30a, a system timing generation circuit 31 for generating a system control signal from the system clock signal to supply the system clock signal and the system control signal to the timing signal generation circuit 33.

[0053] The structure of the imaging apparatus of the fifth embodiment is substantially the same as that of the first embodiment. The difference is that the transmission interval determining circuit 26e is added and the communication control circuit 11 is replaced with the system timing generation circuit 31. A display 32 may be further provided. The timing signal generation circuit 33 includes a driving timing signal generation circuit 27 for the drive circuit 25 and the imager 21, a signal processing timing signal generation circuit 28 for the pre-processing circuit 22, the a/d converter 23, and the signal processing circuit 24, and a transmission timing signal generation circuit 29 for the communication circuit 26.

[0054] The basic operations of the imager 21, the pre-processing circuit 22, the a/d converter 23, the signal processing circuit 24, the communication circuit 26, and the timing signal generation circuit 33 are similar to those of the first embodiment. The difference is that the transmission interval determining circuit 26e obtains a data rate and obtains (right of) a channel of isochronous data and the system timing generation circuit 31 generates the system control signal indicative of a transmission interval.

[0055] Figs. 9A to 9C are timing charts of the fifth embodiment which are also referred in the seventh embodiment. Fig. 10A depicts a flow chart of the transmission interval determining circuit 26e and Fig. 10B depicts a flow chart of the system timing generation circuit 31.

[0056] The transmission interval determining circuit 26e detects the data rate, a communication start timing, a data length of a packet from the transmission and receiving circuit 26c. More specifically, the transmission interval determining circuit 26c obtains the data rate in step ST21. In the following step ST22, the transmission interval determining circuit 26e obtains one of channels of isochronous data (obtains the right of one channel). Then, the transmission interval determining circuit 26e calculates intervals T1 and T2 in step ST23 and sends the data of intervals T1 and T2 to the system timing generation circuit 31.

[0057] The system timing generation circuit 31 generates the system control signal as follows:

[0058] In step ST24, the system timing generation cir-

cuit 31 checks whether the cycle start packet CSP is transmitted by checking the transmission/receiving circuit 26c. If there is a cycle start packet CSP is present, as shown in Fig. 9B, the system timing generation circuit 31 makes the logic level of the system control signal to L after the cycle start packet CSP by the interval T1 in step ST25 and then, after the cycle start packet CSP by the interval T2, the system timing generation circuit 31 makes the logic level of the system control signal to H in step ST26. The system timing generation circuit 31 supplies the system control signal and the system clock signal to the timing signal generation circuit 33.

[0059] As shown in Fig. 9A, it is assumed that the transmission interval determining circuit 26e obtains the channel CH2, the transmission interval determining circuit 26e calculates the interval T1 from the cycle start packet CSP to the beginning of the channel CH2 and the transmission interval determining circuit 26e calculates the interval T2 from the data rate and the data length. Then, the timing signal generation circuit 31 generates the timing signals for intervals T3, T5, and T7. On the other hand, for the interval T4, the timing signal generation circuit 31 does not generates the timing signals for the imager 21, the pre-processing circuit 22, the a/d converter 23, the signal processing circuit 24, and the transmission circuit 26a but the system timing generation circuit 31 continuously monitors the cycle start packet for the interval T4. When a cycle header error occurs, that is, the cycle start packet CSP cannot be detected or a data error occurs in the header of the cycle start packet CSP at t1, the system control signal remains H logic level until the next cycle start packet CSP1 as shown in Fig. 9B.

[0060] As mentioned, the operations of the imager 21, the pre-processing circuit 22, the a/d converter 23, the signal processing circuit, and the transmission circuit 26a are stopped and effected only for the transmission interval, so that the video data is transmitted only for the transmission intervals as shown in Fig. 9C. Accordingly, a power consumption is reduced and undesired electromagnetic emission is suppressed.

[0061] The transmission stop interval may be informed by the display 32.

<SIXTH EMBODIMENT>

[0062] Fig. 11 is a block diagram of the imaging apparatus of a sixth embodiment.

[0063] The structure of the imaging apparatus of the sixth embodiment is substantially the same as that of the fifth embodiment. The difference is that a shutter control circuit 25a is further provided.

[0064] If the communication error occurs, the shutter interval will be extended because the shutter interval is controlled in accordance with the number of pulses of the clock signals or the cycle start packet. To prevent the extension of the shutter interval, when the system timing generation circuit 31 detects the communication error, the communication control circuit 11 operates the shutter control circuit 25a to control a shutter interval of the imager 1 toward a predetermined shutter interval. More specifically, when the communication error is detected because the clock signal cannot be detected, a count value of a counter (not shown) in the shutter interval control circuit 25a for counting pulses of the system clock 30a from the system timing generation circuit 31 may be increased by a predetermined value to make the shutter interval constant. Moreover, it is also possible that a set value to the counter to be compared with the count value in the counter may be decreased by a predetermined value to make the shutter interval constant. Moreover, it is also possible that in response to start of exposure, a timer (not shown) in the shutter interval control circuit 25a measures a predetermined interval and the shutter closing timing is determined in accordance with either the timer or the counter which becomes the shutter closing timing earlier to make the shutter interval constant.

<SEVENTH EMBODIMENT>

[0065] Fig. 12 is a block diagram of the imaging apparatus of a seventh embodiment.

[0066] The structure of the imaging apparatus of the seventh embodiment is substantially the same as that of the fifth embodiment. The difference is that a FIFO memory circuit 34 and a FIFO reading/writing timing signal generation circuit 35 are further provided.

[0067] When there is no communication error, the digital video signal from the signal processing circuit 24 is immediately supplied to the transmission circuit 26a through the FIFO memory circuit 34 during the transmission intervals. On the other hand, during transmission stop intervals; the system timing generation circuit 31 operates the FIFO reading/writing timing signal generation circuit 35 to temporally store the digital video signal from the signal processing circuit 24. If a communication error occurs during transmission stop interval and then, the communication error eliminates, the system timing generation circuit 31 operates the FIFO reading/writing timing signal generation circuit 35 to read the stored the digital video signal to supply the read digital video signal to the transmission circuit 26a to transmit the digital video signal to the transmission line 12.

[0068] As mentioned, if the communication error occurs at t1 as shown in Fig. 9A, the imager 21, the pre-processing circuit 22, the a/d converter 23, the signal processing circuit 24, and the FIFO memory circuit 34 are operated, so that the image represented by the digital video data is temporally stored and transmitted in response to detection of the next cycle start packet CSP1 as shown in Fig. 9A.

[0069] If the communication error occurs because the clock signal cannot be detected by the clock signal detection circuit 6d, the PLL circuit 10 generates the system clock signal 10a at a lowest frequency, so that it is

desirable that the shutter interval control circuit 5a mentioned in the sixth embodiment is provided.

[0070] As mentioned. transmission of video data is stopped when the timing data is not detected from the transmission line 12 or a transmision error occurs, so that it is possible to prevent generation of noise or disturbance in the reproduced image. Moreover, the system control signal indicating the transmission interval is generated from the data rate from the transmission line and the obtained channel, so that the video data is transmitted only for the transmission possible interval, so that a power consumption is reduced and undesired electromagnetic emission is suppressed.

Claims

1. An imaging apparatus comprising:

   imaging means (1, 5);
   optical means (1a) for receiving and forming an image on said imaging means which generates an image signal from said image;
   a/d converting means (3) for a/d-converting said image signal;
   signal processing means (4) for processing said image signal from said a/d converting means to generate a digital video signal;
   communication means (6) for transmitting said digital video signal to a transmission line and receiving a clock signal and timing data transmitted through said transmission line, said timing data indicating a communication timing;
   clock signal detection means (6d) for detecting said clock signal received by said communication means;
   timing signal generation means (7-10) for generating timing signals from said detected clock signal to control said imaging means, said a/d converting means, said signal processing means, and said communication means; and
   communication control means (11) for detecting a communication timing from said timing data, judging whether said communication timing is detected within a predetermined condition, and controlling said timing signal generation means to stop transmitting said digital video signal when said communication timing is not detected within said predetermined condition.

2. An imaging apparatus as claimed in claim 1, wherein said communication means receives a communication cycle header as said timing data and said communication control means detects an error in said communication cycle header from said communication means and judges that said communication timing is not received within said predetermined condition when said error is detected.

3. An imaging apparatus according to claim 1 or 2, wherein said communication control means controls said timing signal generation means to stop operations of said imaging means, said a/d-converting means, said signal processing means, and said communication means when said communication timing is not detected within said predetermined condition.

4. An imaging apparatus according to claim 1, 2 or 3, further comprising shutter controlling means for controlling a shutter interval of said imaging means in accordance with said detected clock signal when said communication timing is detected within said predetermined condition and controlling said shutter interval of said imaging means in response to said detected error toward a predetermined shutter interval.

5. An imaging apparatus according to any one of claims 1 to 4, further comprising storing means for storing said digital video signal, wherein said communication control means operates said storing means to read said digital video signal to supply said digital video signal from said storing means to said communication means when said communication control means judges that the communication timing is not detected within the predetermined condition and then, judges that said communication timing is received again within said predetermined condition.

6. An imaging apparatus according to any one of claims 1 to 5, further comprising display means, wherein said communication control means operates said display means to inform that said communication control means judges said communication timing is not received within said predetermined condition

7. An imaging apparatus comprising:

   imaging means (1);
   optical means (la) for receiving and forming an image on said imaging means which generates an image signal from said image;
   a/d converting means (3) for a/d-converting said image signal;
   signal processing means (4) for processing said image signal from said a/d converting means to generate a digital video signal;
   communication means (6) for transmitting said digital video signal to a transmission line which transmits timing data indicative of a communication cycle and a clock signal, said communication means receiving said timing data and said clock signal;
   clock signal detection means (6d) for detecting

said clock signal received by said communication means;
timing signal generation means (7-10) for generating timing signals from said detected clock signal to control said imaging means, said a/d converting means, said signal processing means, and said communication means; and
data transmission interval signal generation means for detecting a communication timing from said timing data and generating a transmitting interval signal indicative of a transmitting interval and a transmitting stop interval, wherein said communication means transmits said digital video signal only for said transmitting interval.

8. An imaging apparatus as claimed in claim 7, wherein said data transmission interval signal generation means detects transmission data rate data and channel data from said communication means to generate said transmitting interval signal.

9. An imaging apparatus as claimed in claim 7 or 8, wherein said timing signal generation means stops generating said timing signals to stop operations of said imaging means, said a/d-converter, said signal processing circuit, and said transmitting circuit during said transmitting stop interval.

10. An imaging apparatus as claimed in claim 7, 8 or 9, further comprising shutter interval control means for controlling a shutter interval of said imaging means toward a predetermined interval during said transmitting stop interval.

11. An imaging apparatus as claimed in claim 7, 8, 9 or 10, further comprising storing means responsive to said transmission interval signal for storing said digital video signal for said transmission stop interval and reading and supplying said digital video signal to said communication means for said transmission interval.

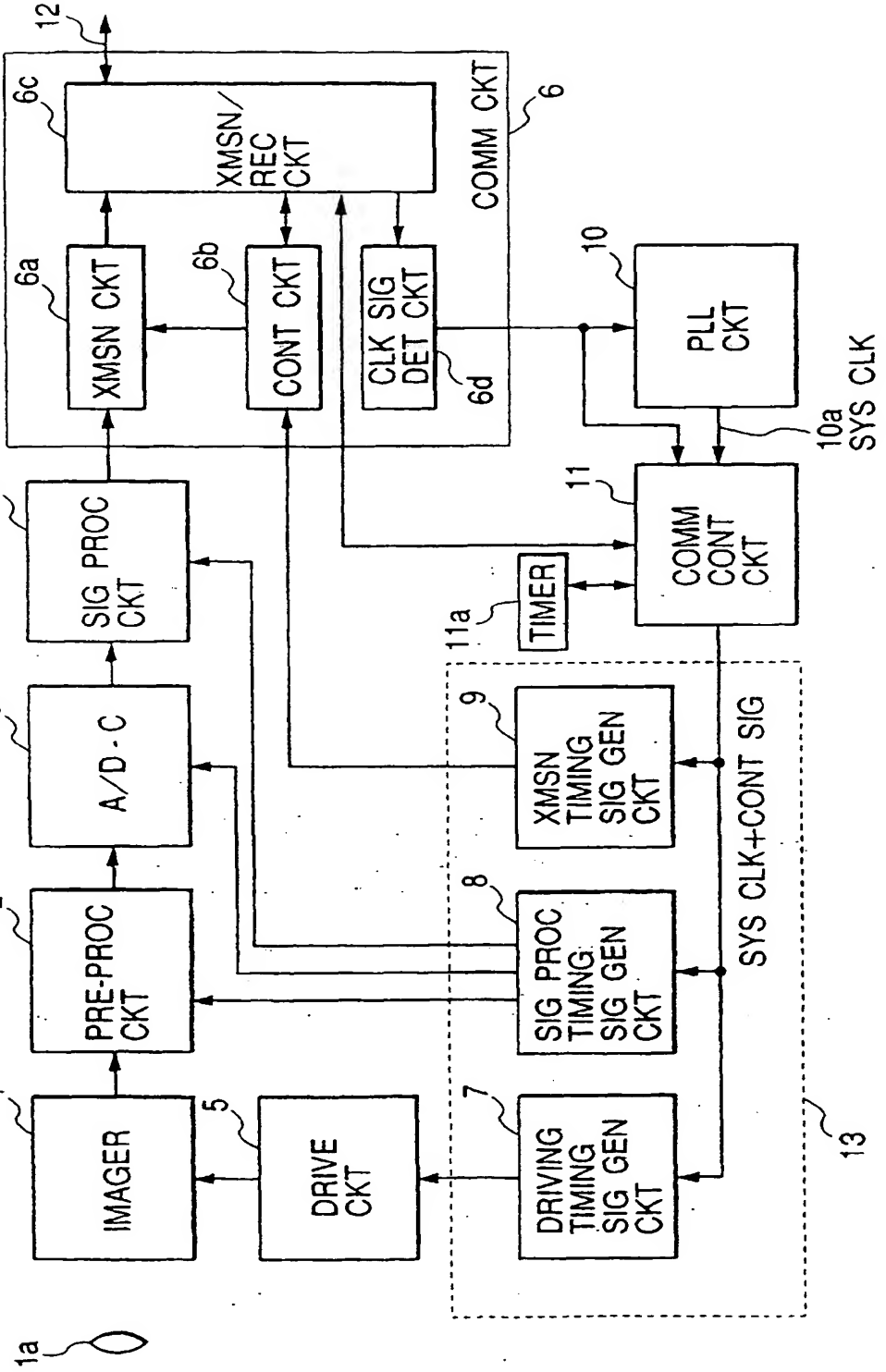
12. An imaging apparatus according to any one of claims 7 to 11 comprising display means for informing that it is during said transmission stop interval.

13. An imaging apparatus as claimed in claim 1, wherein said communication control means detects an error in said communication means, and controls said timing signal generation means to stop transmitting said digital video signal in the presence of said error.

14. An imaging apparatus as claimed in claim 13, wherein said communication control means judges whether said said clock signal is detected within a reference condition to detect said error, and controls said timing signal generation means to stop transmitting said digital video signal in the presence of said error.

15. An imaging apparatus as claimed in claim 13, wherein said communication control means detects a communication timing from said timing data, judging whether said communication timing is detected within a predetermined condition to detect said error, and controlling said timing signal generation means to stop transmitting said digital video signal in the presence of said error.

FIG. 1



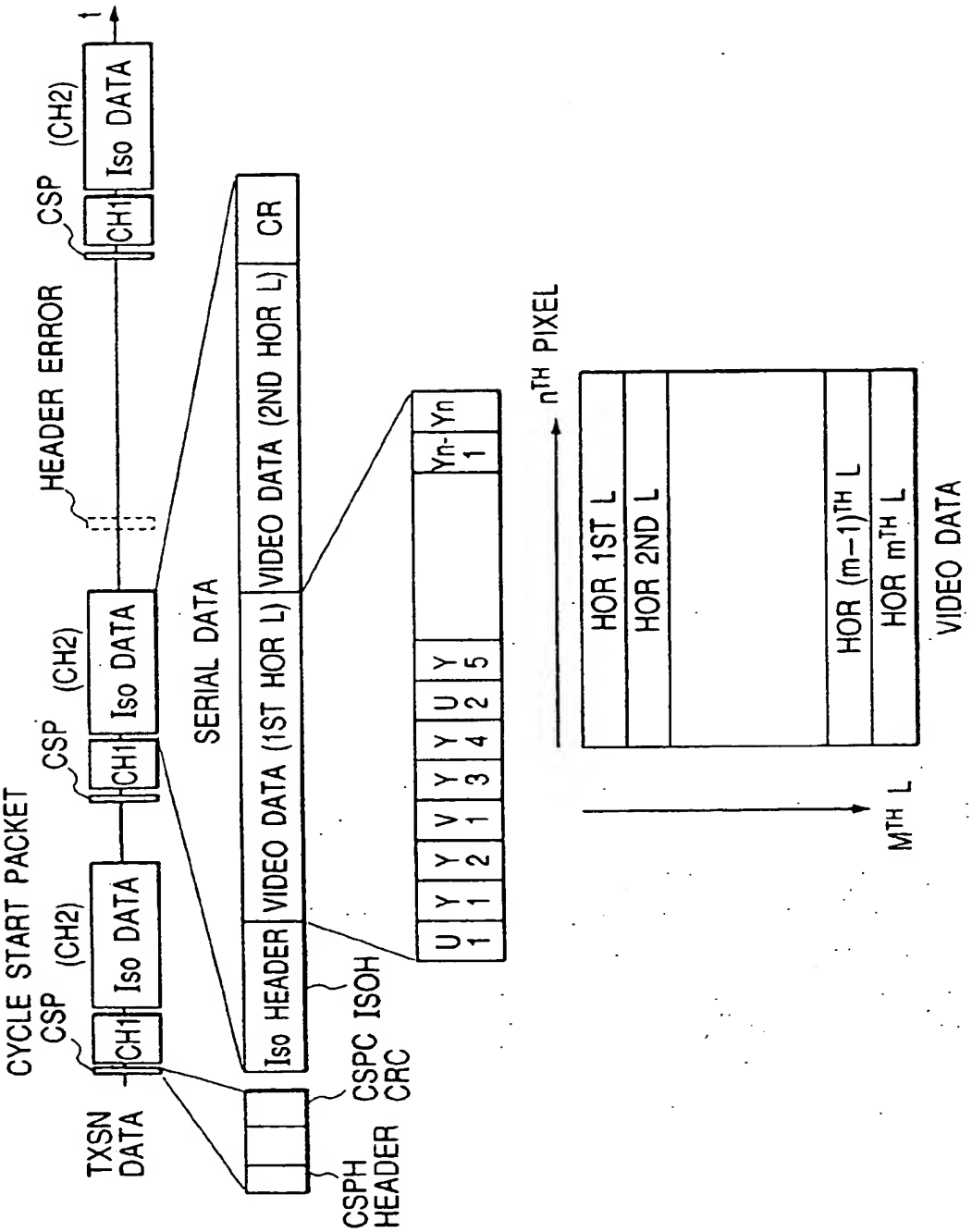


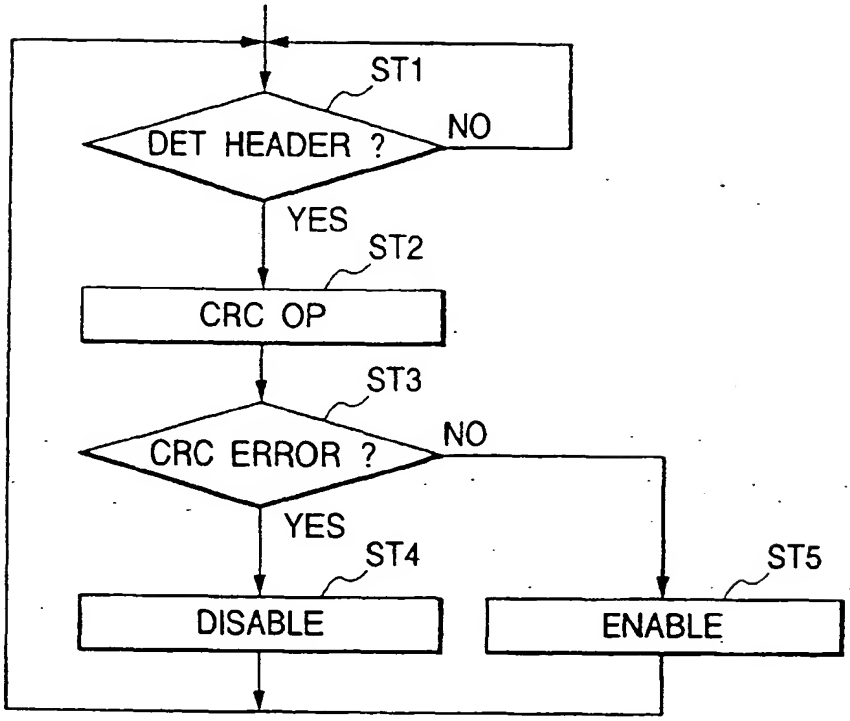
FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

FIG. 3



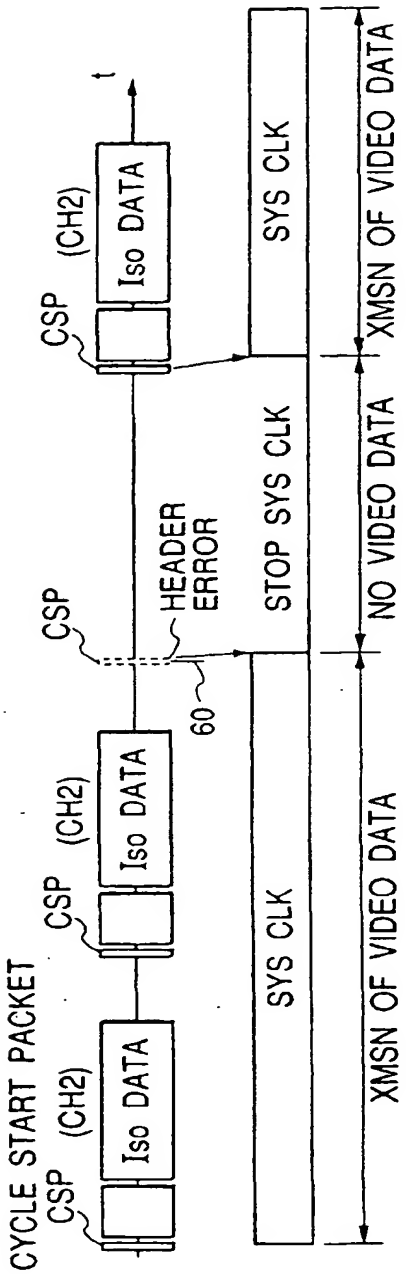

CYCLE START PACKET
CSP
(CH2)
Iso DATA
CSP
(CH2)
Iso DATA
CSP
(CH2)
Iso DATA
CSP
HEADER ERROR
60
CSP
(CH2)
Iso DATA
t
TXSN DATA
SYS CLK
STOP SYS CLK
SYS CLK
XMSN OF VIDEO DATA
NO VIDEO DATA
XMSN OF VIDEO DATA

FIG. 4A

FIG. 4B

FIG. 5

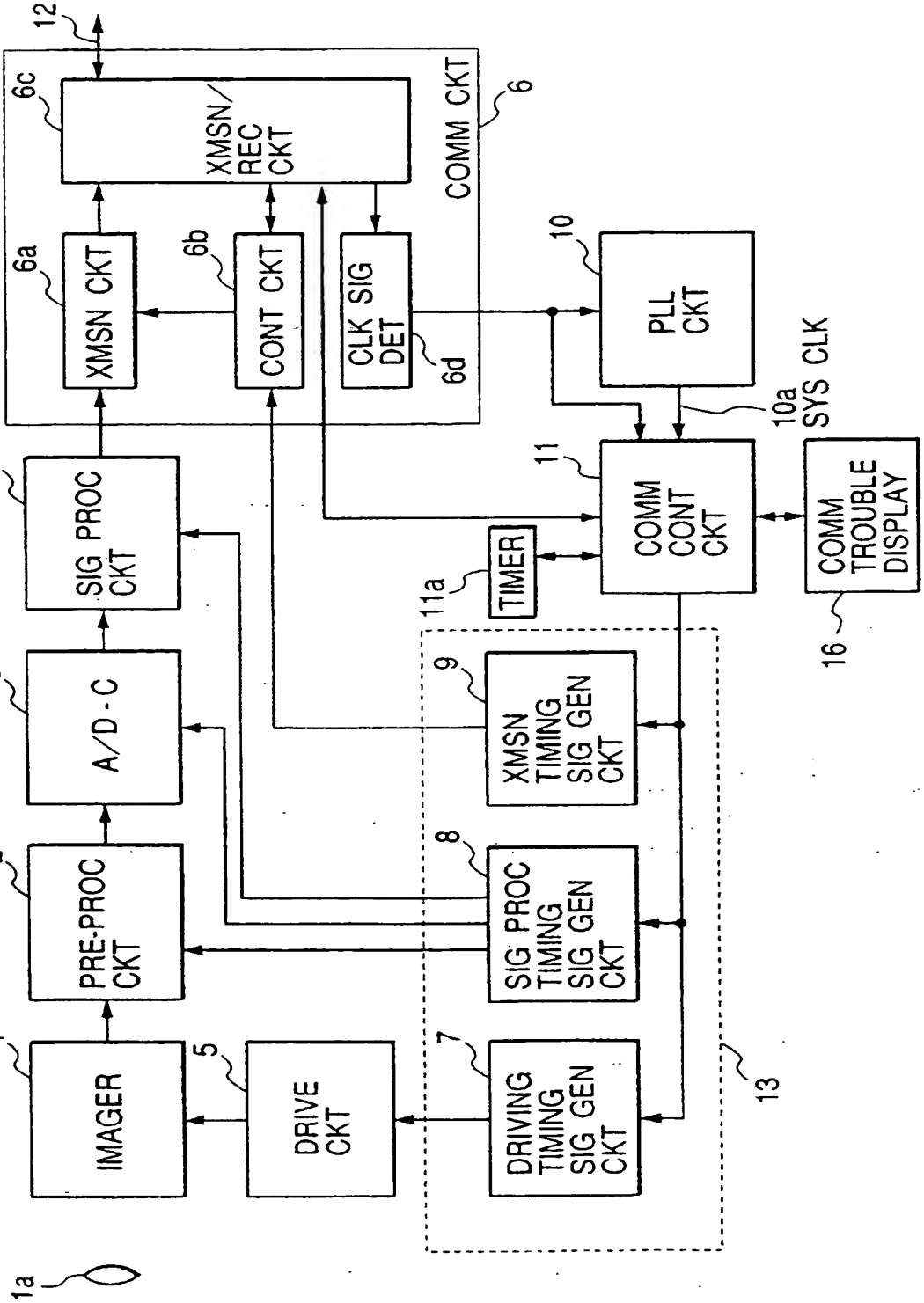


FIG. 6

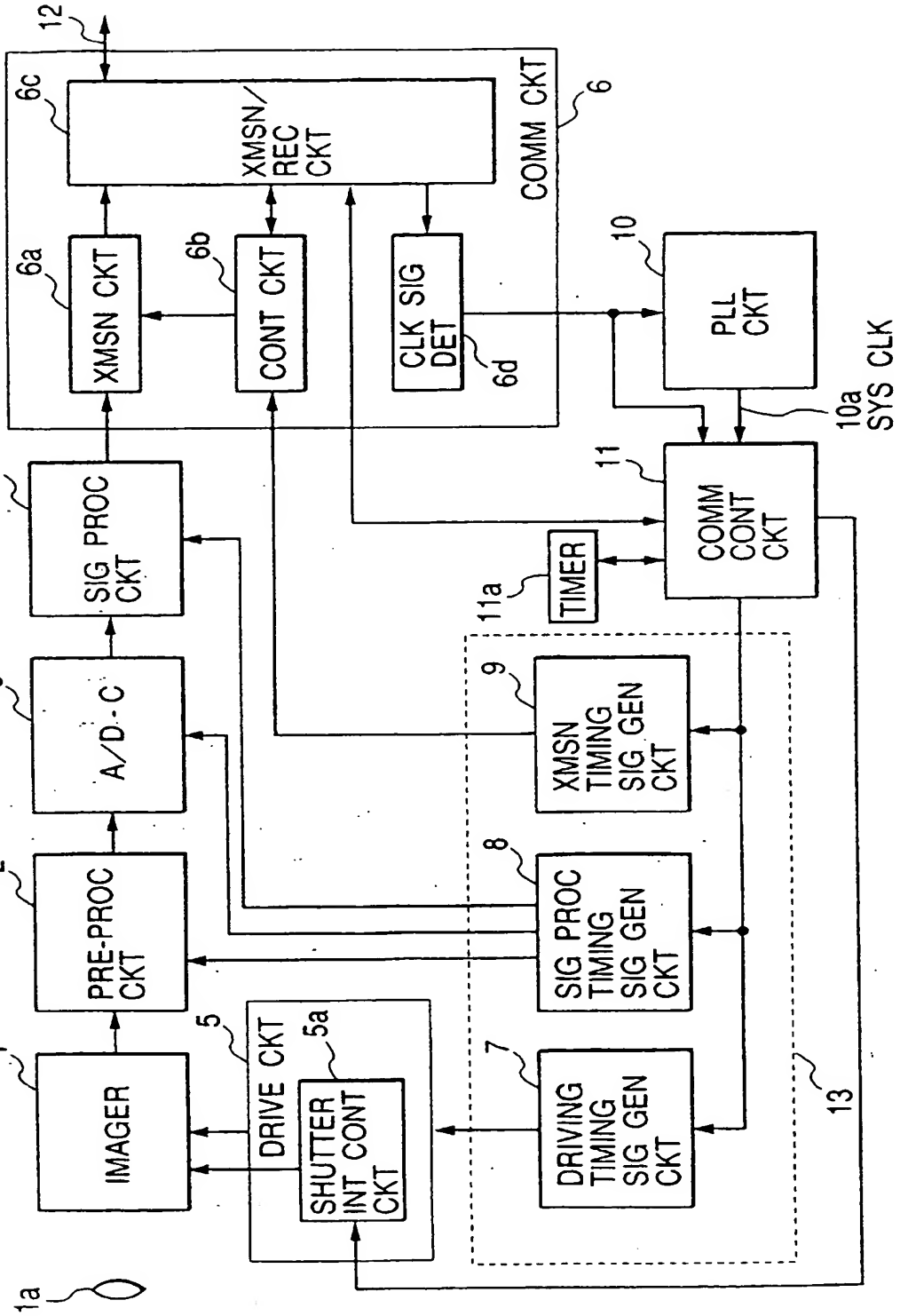

1a
1
IMAGER
2
PRE-PROC CKT
3
A/D-C
4
SIG PROC CKT
5
DRIVE CKT
5a
SHUTTER INT CONT CKT
6
COMM CKT
6a
XMSN CKT
6b
CONT CKT
6c
XMSN/ REC CKT
6d
CLK SIG DET
7
DRIVING TIMING SIG GEN CKT
8
SIG PROC TIMING SIG GEN CKT
9
XMSN TIMING SIG GEN CKT
10
PLL CKT
10a
SYS CLK
11
COMM CONT CKT
11a
TIMER
12
13

FIG. 7

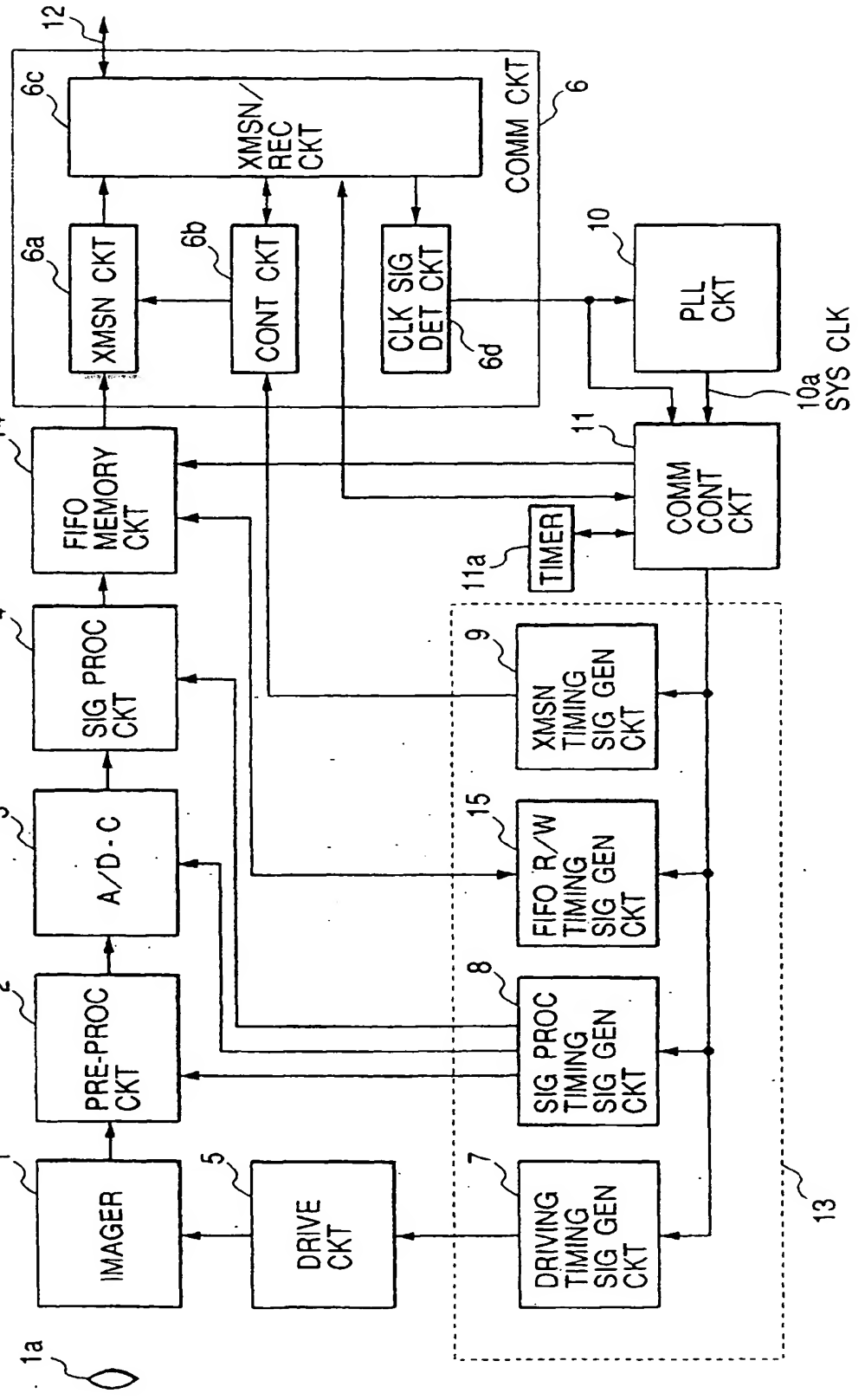
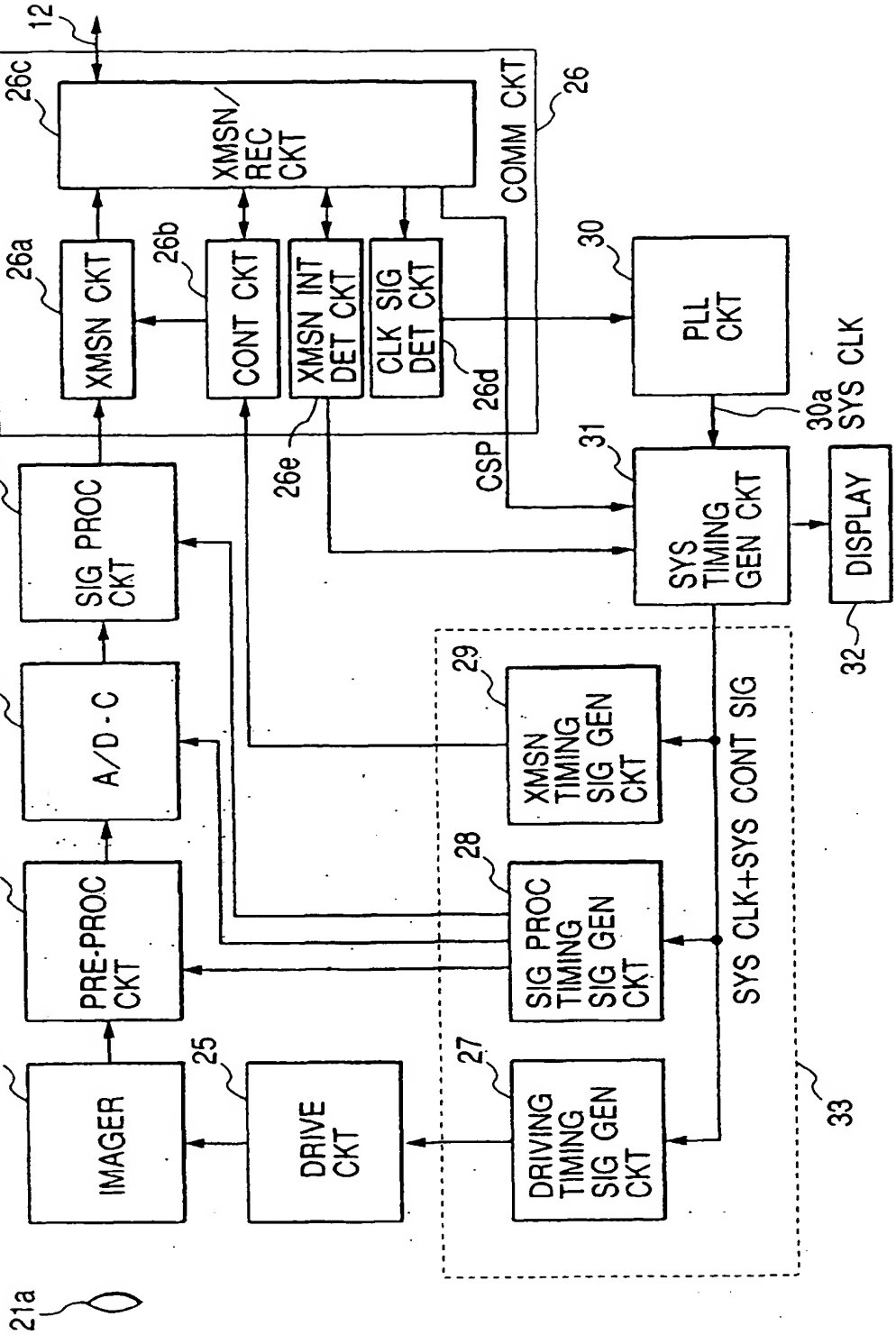


FIG. 8



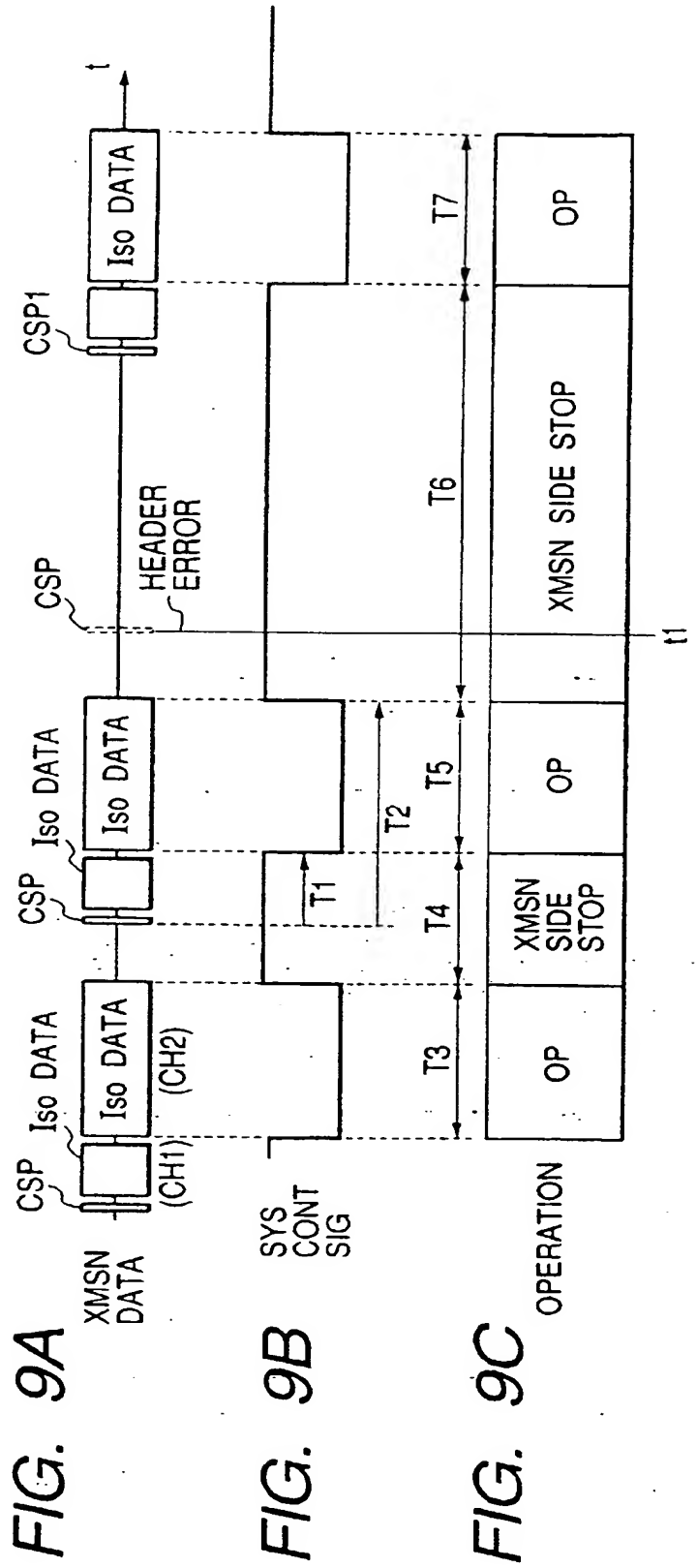


FIG. 9A

FIG. 9B

FIG. 9C

FIG. 10A

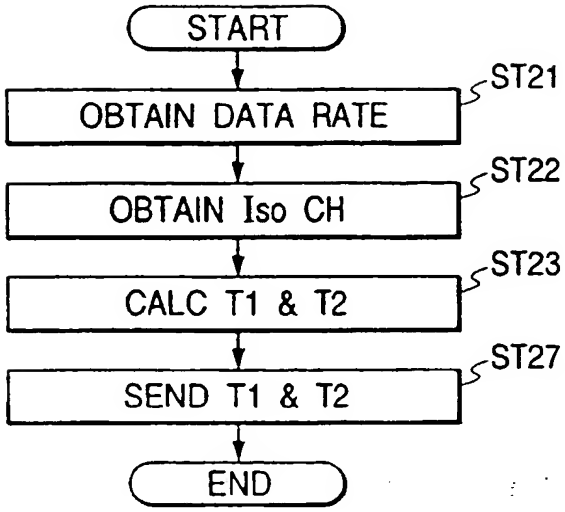


FIG. 10B

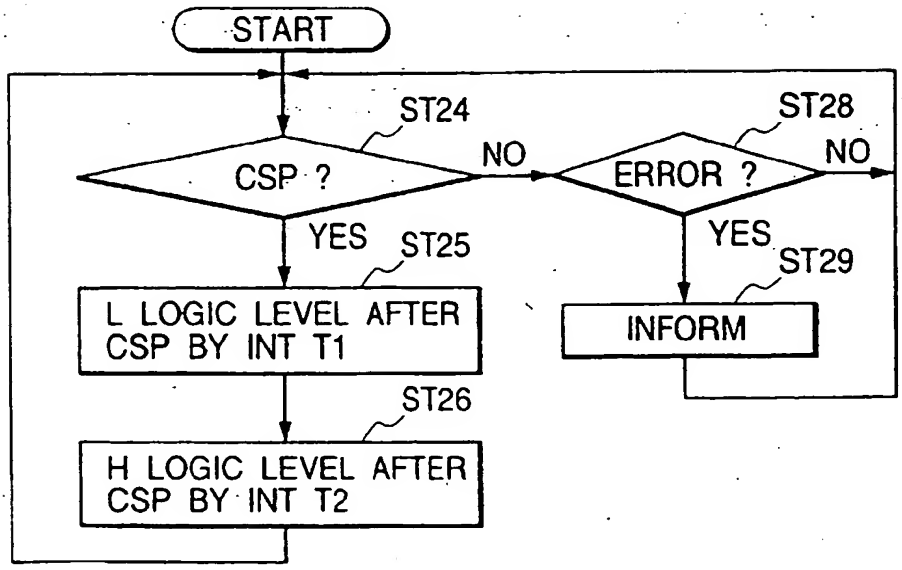


FIG. 11

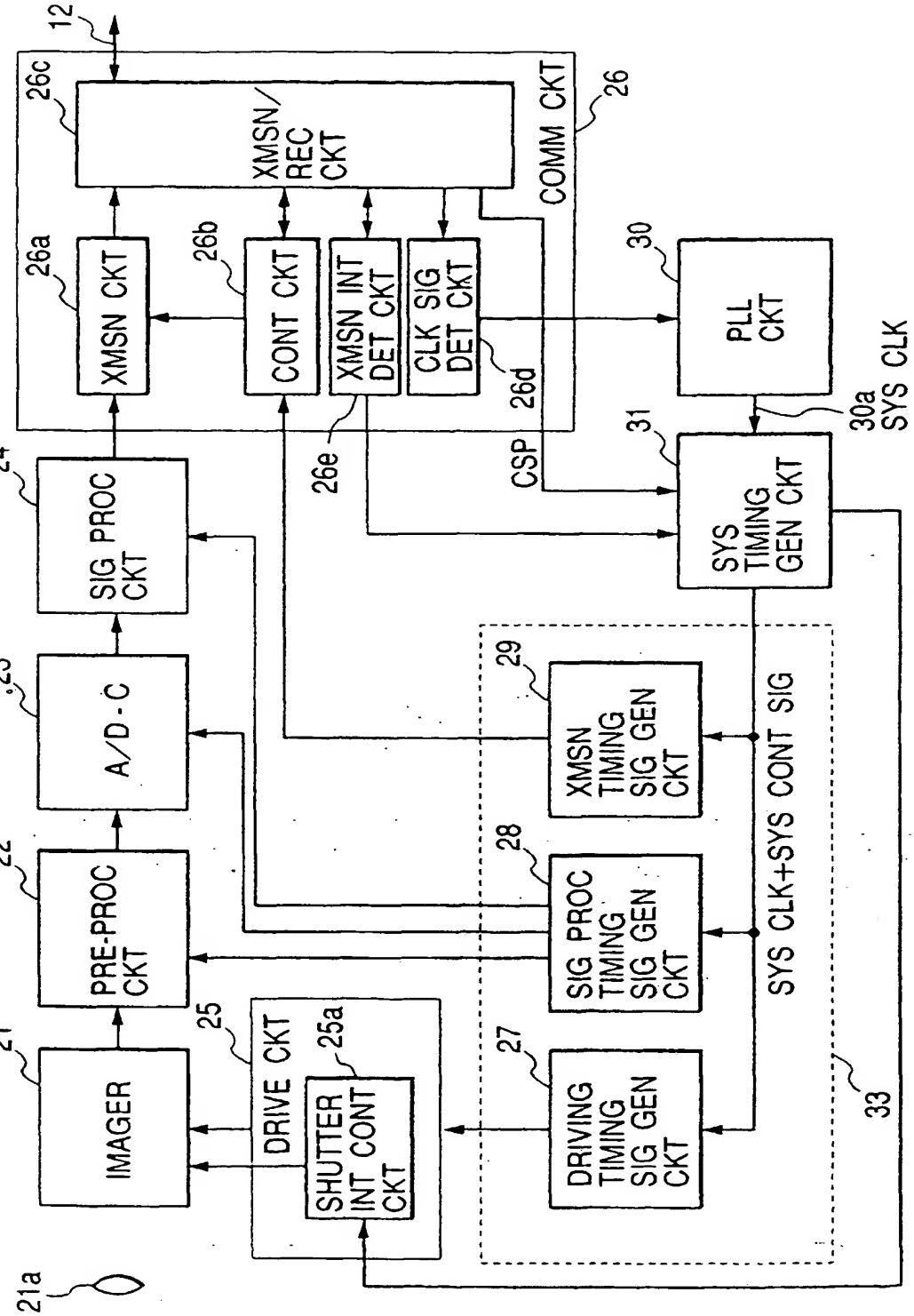


FIG. 12

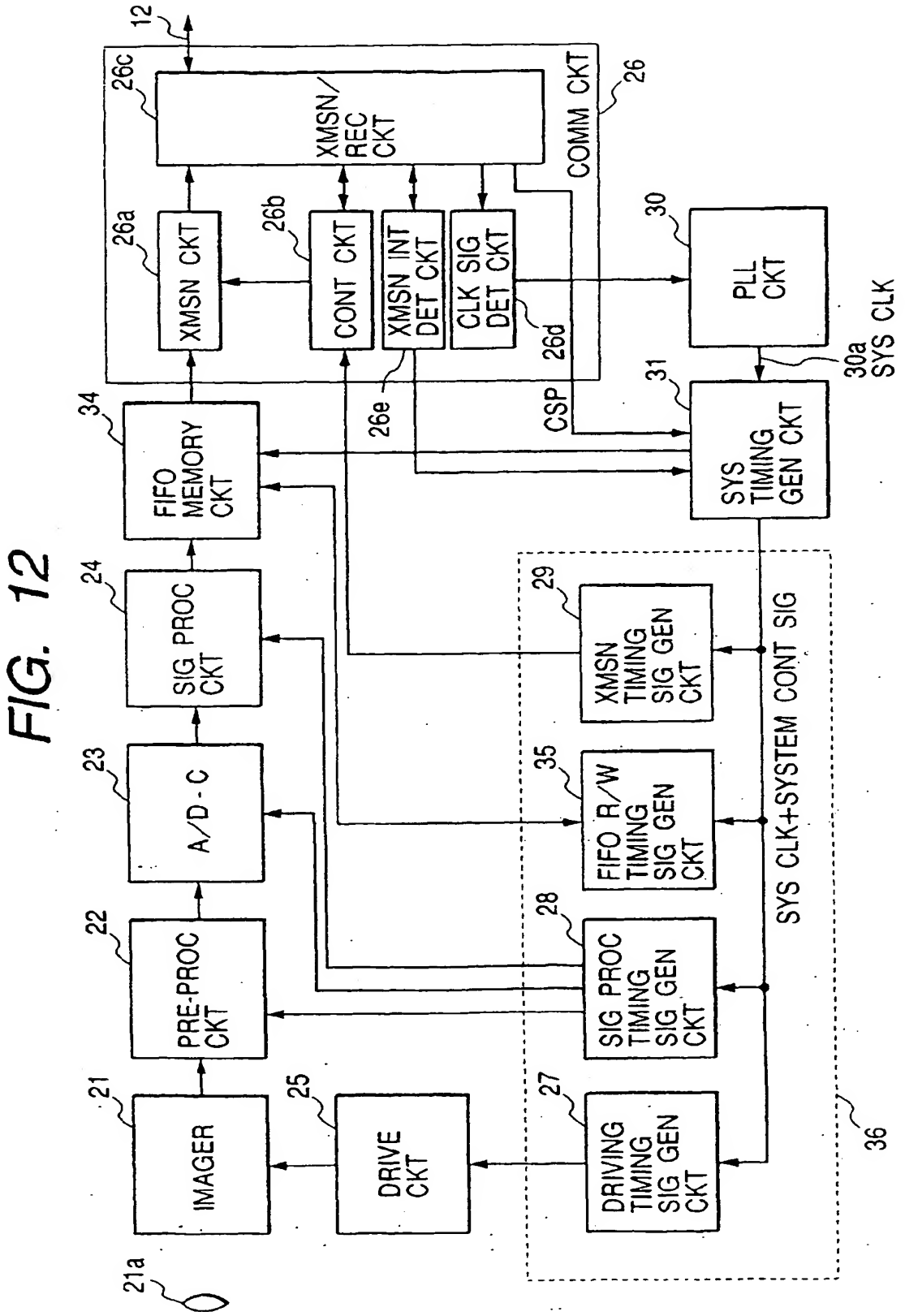
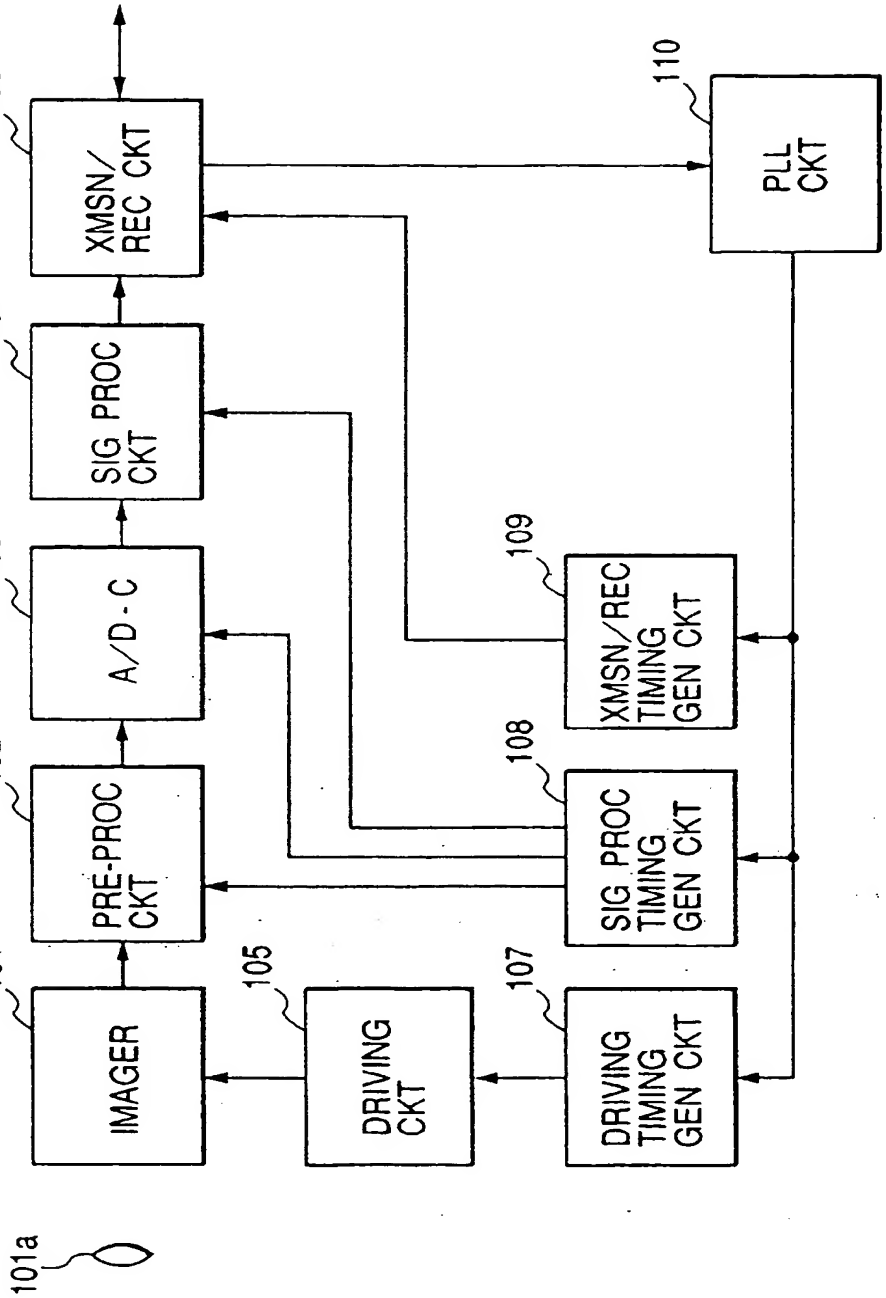

12
26c
XMSN/
REC
CKT
COMM CKT
26
26a
XMSN CKT
26b
CONT CKT
XMSN INT
DET CKT
CLK SIG
DET CKT
26d
30
PLL
CKT
30a
SYS CLK
34
FIFO
MEMORY
CKT
26e
CSP
31
SYS
TIMING
GEN CKT
24
SIG PROC
CKT
29
XMSN
TIMING
SIG GEN
CKT
23
A/D - C
35
FIFO R/W
TIMING
SIG GEN
CKT
22
PRE-PROC
CKT
28
SIG PROC
TIMING
SIG GEN
CKT
SYS CLK+SYSTEM CONT SIG
21
IMAGER
25
DRIVE
CKT
27
DRIVING
TIMING
SIG GEN
CKT
36
21a

FIG. 13
PRIOR ART



(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 991 268 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
27.03.2002 Bulletin 2002/13

(43) Date of publication A2:
05.04.2000 Bulletin 2000/14

(21) Application number: **99307645.4**

(22) Date of filing: **28.09.1999**

(51) Int Cl.[7]: **H04N 5/232**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.09.1998 JP 27401198**

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka 571-8501 (JP)

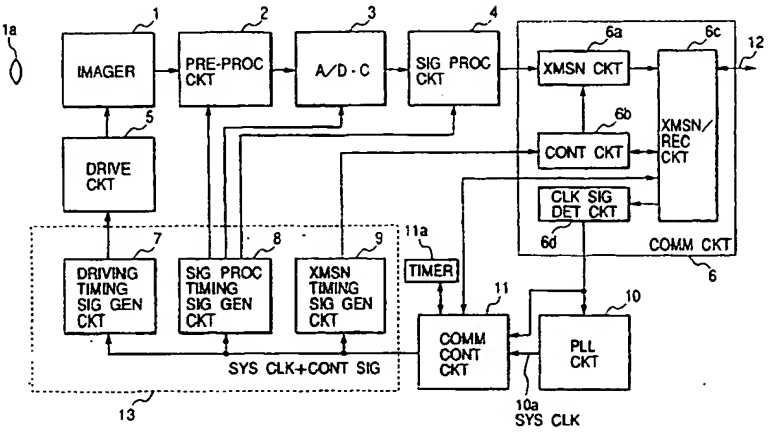
(72) Inventor: **Shinohara, Toshiaki**
Oomiya-shi, Saitama-ken 330-0038 (JP)

(74) Representative: **Senior, Alan Murray et al**
J.A. KEMP & CO.,
14 South Square,
Gray's Inn
London WC1R 5JJ (GB)

(54) An imaging apparatus with video data transmission

(57) A communication circuit transmits the digital video signal to a transmission line and receives a clock signal and timing data transmitted through the transmission line. The timing data indicates a communication timing. A timing signal generation circuit generates timing signals from the detected clock signal to control the imager, the a/d converting circuit, the signal processing circuit, and the communication circuit. A communication control circuit detects a communication timing from the timing data, judges whether the communication timing is detected within a predetermined condition (communication error), and controls the timing signal generation circuit to stop transmitting the digital video signal when the communication timing is not detected within the predetermined condition to prevent a fail in transmitting the video data. A shutter interval of the imager is further controlled toward a constant shutter interval in response to the communication error. The video signal is stored in a memory in response to the communication error and read if the communication error eliminated. The communication error is displayed. A system control signal indicative of data transmission period is generated in response to a received cycle start packet in accordance with the obtained data rate and channel timing.

FIG. 1



EP 0 991 268 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 7645

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	EP 0 522 794 A (SONY CORP) 13 January 1993 (1993-01-13) * column 1, line 14 - line 27 * ---	1,7	H04N5/232
A	EP 0 777 381 A (CANON KK) 4 June 1997 (1997-06-04) * column 7, line 9 - line 54 * ---	1,7	
A	EP 0 740 475 A (SONY CORP) 30 October 1996 (1996-10-30) * column 2, line 27 - line 40 * ---	1,7	
A	US 5 608 490 A (OGAWA HIDEHIRO) 4 March 1997 (1997-03-04) * column 2, line 24 - line 58 * -----	1,7	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	6 February 2002	Bequet, T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 7645

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

06-02-2002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0522794 A	13-01-1993	JP 3030946 B2	10-04-2000
		JP 5252448 A	28-09-1993
		DE 69218505 D1	30-04-1997
		DE 69218505 T2	31-07-1997
		EP 0522794 A1	13-01-1993
		KR 263696 B1	01-08-2000
		US 5387932 A	07-02-1995
EP 0777381 A	04-06-1997	JP 9161048 A	20-06-1997
		JP 9163237 A	20-06-1997
		JP 9163238 A	20-06-1997
		EP 0777381 A2	04-06-1997
EP 0740475 A	30-10-1996	JP 8307649 A	22-11-1996
		EP 0740475 A2	30-10-1996
		US 6219096 B1	17-04-2001
US 5608490 A	04-03-1997	JP 8006099 A	12-01-1996

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82